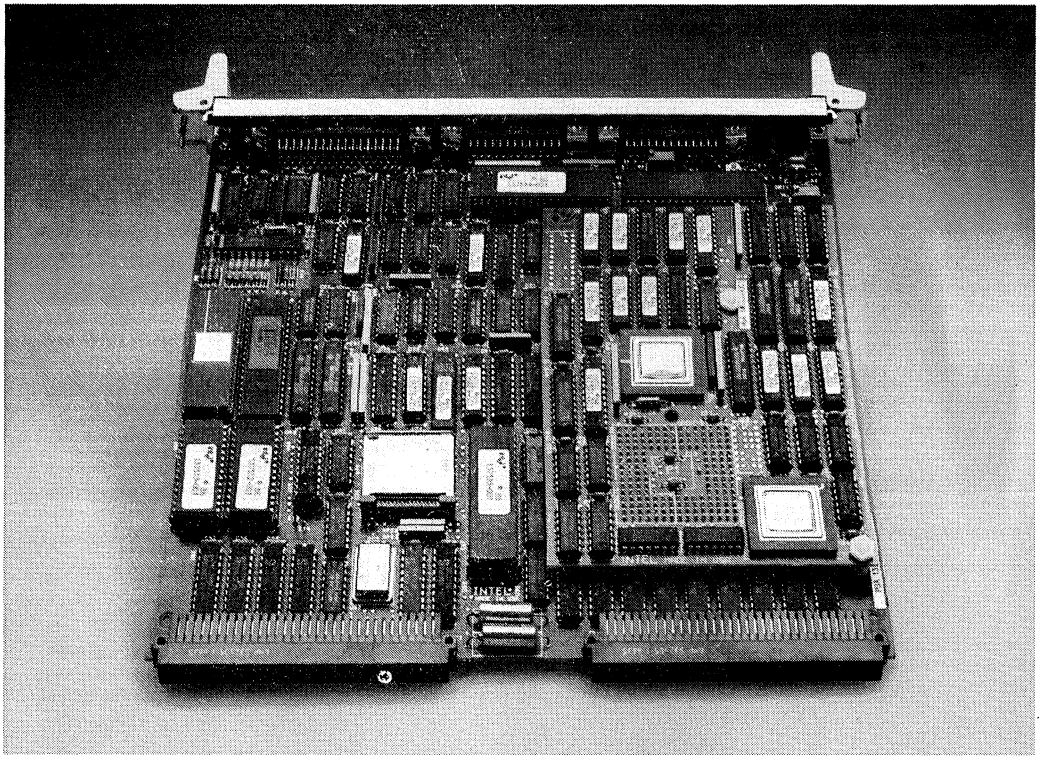
iSBC® 186/224A MULTIBUS® II MULTI-PERIPHERAL CONTROLLER SUBSYSTEM

- **Complete I/O Subsystem for Mass Storage Devices**
- **Based on the 80186 Microprocessor**
- **On-Board Firmware Provides Concurrency of Operation**
- **Controls up to Four ST506/412 Winchester Disk Drives, up to Four SA450/460 Floppy Drives, and up to Four QIC-02 Streaming Tape Drives**
- **128K Bytes of On-Board DRAM Allows Multiple Track Caching for High Speed Winchester Data Access**
- **MPC (Message Passing Coprocessor) Single Chip Interface to the Parallel System Bus With Full Message Passing**
- **Software Configurability: Geographic Addressing**
- **Built-In-Self-Test (BIST) Diagnostics On-Board**

The iSBC 186/224A Multi-Peripheral Controller Subsystem supports the full Message Passing protocol of the MULTIBUS II System Architecture and provides peripheral I/O control for a wide variety of OEM applications. The iSBC 186/224A controller serves as a complete peripheral I/O subsystem and supports the predominant types of storage media: Winchester disks, floppy disks, and quarter-inch streaming tapes. On-board firmware for the board provides improved Winchester disk operation through multiple data track caching. This subsystem capability is provided on a single 8.7 x 9.2 inch double-high Eurocard form factor printed circuit board.



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ARCHITECTURE

Dual-Bus Architecture On-Board

The iSBC 186/224A controller is designed around a dual bus structure and is supported by real-time, multitasking firmware. The dual bus structure consists of the local bus and the I/O transfer bus. This dual-bus approach offers maximum task concurrency—allowing the 80186 CPU to execute code and/or manipulate data during data transfers to and from the various storage media.

The iSBC 186/224A controller uses the MULTIBUS II Parallel System Bus (iPSB) to transfer commands and data to requesting or sending agents and can send and receive both solicited and unsolicited messages as specified in the MULTIBUS II Bus Architecture Specification Handbook. (See Figure 1 for functional block diagram of the 186/224A board).

The local bus consists of the 80186 microprocessor, the EPROM MPC (for access to the iPSB), and interrupt control. The 80186 component controls the local bus and manages the interface between the iPSB and the controller. DMA channels internal to the 80186 are used for data transfers between on-board memory and the MPC.

The I/O Transfer bus supports data transfers between the iSBC 186/224A controller and the various peripheral devices. The Winchester, floppy, and tape interfaces reside on the I/O Transfer bus as do the DMA controller, track cache DRAM, and local bus arbitration logic.

The 8237A-5 DMA controller directly controls four independent DMA channels and provides the capability for performing time-multiplexed, concurrent data transfer operations between the respective device interfaces and the local DRAM.

A total of 128K bytes of zero wait state DRAM is provided on-board. This DRAM is local to the I/O Transfer bus. It is accessible to both the CPU and the DMA controller. It supports the 80186 stack and interrupt vectors and 64K bytes of Winchester track cache. The DRAM is configured for 16-bit (word) access but also supports byte-swapping.

This dual-bus architecture combined with the real-time control firmware and PCI command protocol allows the concurrent transfer of data between multiple storage devices and the controller and between the controller and the MULTIBUS II Parallel System Bus resulting in improved system level performance.

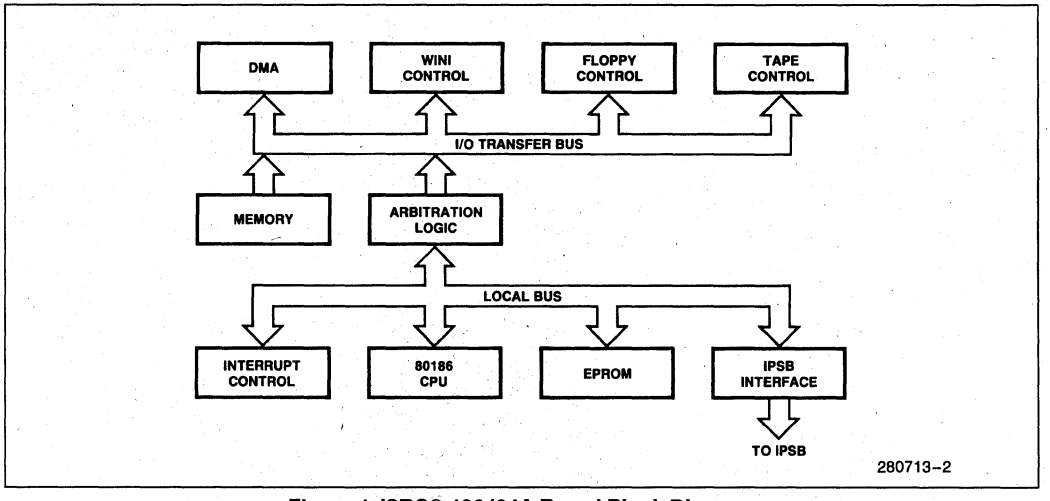

Figure 1. iSBC® 186/24A Board Block Diagram

Interconnect Space Subsystem

MULTIBUS II Interconnect Space is a standardized set of software configurable registers designed to hold and control board configuration information as well as system and board level diagnostics and testing information. Interconnect space is implemented with the 8751 microcontroller and the MPC bus interface silicon.

The read-only registers store information such as, board type, vendor I.D., firmware revision level, etc. The software configurable registers are used for controller options, identifying certain device characteristics, and diagnostics.

Built-In-Self-Test Diagnostics

On-board built-in-self-test (BIST) diagnostics provides confidence testing of the various functional areas of the iSBC 186/224A controller board. The initialization checks are performed by the 8751 microcontroller, while the BIST package is executed by the 80186 microprocessor.

BIST provides valuable testing and error reporting and recovery capability on MULTIBUS II boards, enabling the OEM to reduce manufacturing and maintenance costs. An LED on the board's front panel indicates the status of power-up diagnostics.

PCI Peripheral Communications Interface

PCI is a logical message-based peripheral controller interface to provide a standard software interface on peripheral I/O boards. This protocol provides a vehicle to issue multiple commands or statuses concurrently. This allows the 186/224A board to accept multiple commands and queue them in on-board memory.

BACKPLANE BUS INTERFACES

P1 Connector: This is used as the standard MULTIBUS II 32-bit parallel system bus. It contains all signals required to implement the full standard interface.

P2 Connector: The P2 connector is not electrically connected internally on the board.

Winchester Connections: One 50-pin D-type, right angle female, high density connector which provides all of the required signals for up top four Winchester disk drives.

Flexible Disk Connections: One 25-pin D-type connection which provides all of the required signals for up to four daisy-chained flexible disk drives.

QIC-02 Streaming Tape Connections: One 25 pin D-type connection which provides the required signals for up to four daisy-chained tape drives.

I/O Connectors: The I/O connections for each interface are on the front panel. In order to provide a reliable connection to the peripheral devices, additional ground lines are included at the connector.

SPECIFICATIONS

CPU: 5 MHz 80186 synchronized to 5 MHz 8237A-5 DMA controller

Memory: 128K bytes DRAM on-board for buffers and track cache

2 PROM sites contain Built-in-Self-Test (BIST) and PCI firmware

Mass Storage Device Compatibility

Winchester—Any ST506/412 compatible 5¼" drive.
Manufacturers include: Quantum, CMI, CDC, Maxtor, Memorex, Atasi.
Densities range from 10 MB to 140 MB.

Floppy—Any SA450/460 compatible 5¼" drive.
Manufacturers include: Teac, Shugart.
Sizes include half height, full height, 48TPI, 96TPI.

Tape—Any QIC-02 compatible, ¼" streaming tape drive.
Manufacturers include: Archive, Cipher, Tandberg.

Physical Dimensions

The iSBC 186/224A board meets all the mechanical specifications as presented in the MULTIBUS II specification (order #146077 rev. C).

DOUBLE-EUROCARD FORM FACTOR

Depth: 220 mm (8.6 in)

Height: 233 mm (9.2 in)

Front Panel Width: 20 mm (0.784 in.)

CONNECTORS

Interface	Connector	Part No.
iPSB bus (P1)	96 Pin DIN, Right Angle Female	603-2-IEC-C096-F
P2	96 Pin DIN, Right Angle Female, Not Connected Internally	603-2-IEC-C096-F
ST506/412 (Winchester)	50 Pin D Type, Right Angle Female, High Density (See Note)	
SA450/460 (Floppy)	25 Pin D-Type, Right Angle Female, (See Note)	
QIC-02 (Tape)	25 Pin D-Type, Right Angle Female, (See Note)	

NOTE:
The manufacturers below provide connectors which will plug into the connectors supplied on the iSBC 186/224A board front-panel.

Connector Type	Manufacturer	Pins	Part No.
Flat Ribbon Crimped	T&B Ansley	50	609-50P
	T&B Ansley	25	609-25P
Bulk Cable Solder Cup	Amlan	50	CDS50L
	Amlan	25	CDS25L
	ITT Cannon	50	DD-50P
	ITT Cannon	25	DB-25P
Pin Crimp	AMP	50	206438-1
	AMP	25	205436-1
	ITT Cannon	50	DDC-50P
	ITT Cannon	25	DBC-25P

Reference Manuals

iSBC 186/224A Board Hardware Reference Manual (order number 138272-001)

Intel MULTIBUS II Bus Architecture Specification (order number 146077)

Manual may be ordered from any Sales Representative, Distribution Office, or from the Intel Literature Department, 3065 Bowers Ave., Santa Clara, CA 95051.

ORDERING INFORMATION

Part Number	Description
iSBC 186/224A	Multiperipheral Controller Subsystem